What is claimed is:

1. A micro-leadframe for mounting at least one integrated circuit, comprising:

a flat base having at least one conductive lead pattern to provide electrically conductive paths for said at least one integrated circuit; and

a plurality of preload extension tabs arranged about said at least one conductive lead pattern, the preload extension tabs protruding at an angle with respect to the flat base to a predetermined height above the flat base.

2. The micro-leadframe of claim 1, wherein said at least one integrated circuit is positioned on said at least one conductive lead pattern of the flat base, said at least one integrated circuit comprising a mold cap having a predetermined height above the flat base.

3. The micro-leadframe of claim 2, wherein said at least one integrated circuit package further comprises a semiconductor die within the mold cap.

4. The micro-leadframe of claim 3, wherein the semiconductor die comprises a flipchip die.

5. The micro-leadframe of claim 3, wherein the preload extension tabs are directly connected to the mold cap.

6. A micro-leadframe package, comprising:

a flat base having a conductive lead pattern;

an integrated circuit connected to the conductive lead pattern of the flat base;

a plurality of preload extension tabs arranged about the conductive lead pattern, the preload extension tabs protruding at an angle with respect to the flat base into the integrated circuit package to a predetermined height above the flat base.

7. The micro-leadframe package of claim 6, wherein the integrated circuit comprises a plastic mold cap having a predetermined height above the flat base.

8. The micro-leadframe package of claim 7, wherein the integrated circuit further comprises a semiconductor die within the mold cap.

9. The micro-leadframe package of claim 8, wherein said at least one integrated circuit package further comprises a plurality of flipchip connections between the semiconductor die and the conductive lead pattern.

10. The micro-leadframe package of claim 8, wherein the preload extension tabs are directly connected to the flat base.

11. A method of packaging an integrated circuit, comprising the steps of:

providing a patterned micro-leadframe having a flat base;

forming a plurality of preload extension tabs protruding from the flat base at a predetermined angle with respect to the flat base to a predetermined height above the flat base; and

attaching a mold compound to the micro-leadframe.

12. The method of claim 11, further comprising the step of providing a top mold platten.

13. The method of claim 12, wherein the step of attaching the mold compound to the micro-leadframe comprises the step of heating the top mold platten and forcing the top mold platten against the preload extension tabs.

14. The method of claim 13, further comprising the step of providing a bottom mold platten.

15. The method of claim 14, wherein the step of attaching the mold compound to the micro-leadframe further comprises the steps of heating the bottom mold platten and pressing the bottom mold platten against the patterned flat base.

16. The method of claim 11, wherein the step of forming the preload extension tabs comprises the step of bending the preload extension tabs to the predetermined angle with respect to the flat base.